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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:

Jerrell P. Hein

Application No: 09/502,282

Filed: February 10, 2000

For: SUBSCRIBER LINE INTERFACE CIRCUITRY

Examiner: TIEU, Binh Kien

Art Unit: 2643

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Appellant's Brief Under 35 C.F.R. § 1.192

Applicant (Appellant) respectfully submits this brief in triplicate in support of an appeal from the Examiner's Final Office Action dated December 12, 2003 that finally rejected claims 1-13, 15-27, and 32-36. Appellant respectfully requests consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the above-referenced application.

The Brief is required to be filed within two months from the date of receipt of the Notice of Appeal (MPEP § 512). The Office stamped a receipt date of June 14, 2004 on Appellant's return postcard thus establishing a due date of August 14, 2004. This Appeal Brief is accompanied by a petition and fee for a two month extension of time extending the time period for response to October 14, 2004. Given that this Brief is filed on or before October 14, 2004 as indicated above, appellant respectfully submits this Brief is timely filed in accordance with 37 C.F.R. §§ 1.192, 1.136.

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I. REAL PARTY IN INTEREST

The above-identified application for patent is assigned to Silicon Laboratories, Inc., the real party in interest. Silicon Laboratories, Inc. is a Delaware corporation having a principal place of business at 4635 Boston Lane, Austin, Texas 78735.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any other related appeals or interferences that may directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-36 are pending. Claims 14 and 28-31 were indicated as being allowable if re-written. Claims 1-13, 15-27, and 32-36 stand rejected. In particular, claims 1-13, 15-27, and 32-36 were rejected under 35 U.S.C. § 103 as being unpatentable over various combinations of U.S. Patent No. 6,178,241 of Zhou ("Zhou"), U.S. Patent No. 5,323,460 of Warner ("Warner"), U.S. Patent No. 4,984,266 of Smith ("Smith"), U.S. Patent No. 4,609,781 of Gay ("Gay"), U.S. Patent No. 5,323,460 of Chen ("Chen").

IV. STATUS OF AMENDMENTS

No amendment was submitted in response to the final Office Action.

V. SUMMARY OF THE INVENTION

A subscriber loop interface circuit apparatus includes a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop. The signal processor resides on a same integrated circuit die as a codec for bi-directional communication of voiceband data between the analog

subscriber loop and a digital interface of the signal processor. In one embodiment, the signal processor generates a linefeed driver control signal in response to the sensed signals. In one embodiment, the signal processor calculates the common mode and differential mode components of the subscriber loop. (Specification, p. 3, lines 1-9, 22-25; p. 8, lines 7-16; p. 9, lines 12-18, 23 through p. 10, line 4; Figs. 2, 4)

VI. CHARACTERIZATION OF CITED REFERENCES

Zhou includes a disclosure of a subscriber line interface card. A SLIC (310) senses the tip and ring lines of the subscriber loop. A SLAC (304) converts digital voiceband data from the PCM interface of the line card (308) into analog voiceband data for the subscriber loop. The SLAC also receives analog voiceband data from the SLIC and converts the analog data into digital voiceband data for communication to the PCM interface of the line card. The SLICS and the SLAC are clearly different integrated circuits (Zhou, col. 1, line 53 through col. 2, line 32; col. 3, lines 24-38; col. 5, lines 22-26; Figs. 2-3).

Warner includes a disclosure of a subscriber line interface circuit having a line configuration and protection circuit (LCP 103) and a thick-film hybrid module (XBRID 100). XBRID module 100 includes a high voltage line interface (HVLI 101) and a hybrid combo circuit (HCOMBO 102). The HVLI and HCOMBO form a SLIC. The HVLI is a bipolar monolithic integrated circuit. (Warner, col. 5, lines 31-66; Figs. 1-2) The HCOMBO 102 synthesizes the input impedance of the SLIC and performs hybrid balance echo cancellation. Additionally, the HCOMBO 102 converts the differential audio signals from the HVLI 101 to PCM encoded digital signals and from PCM encoded signals to differential audio signals. (Warner, col. 8, lines 56-63; Figs. 2, 4)

Smith includes a disclosure of an eight line (channel) subscriber line card arrangement where each of the eight subscriber lines is interfaced by a high voltage analog circuit followed by a low voltage circuit. A single CMOS digital

signal processor is multiplexed between each channel to save digital hardware. (Smith col. 2, lines 12-63).

Gay includes a disclosure of a method for adjusting a BORSHT/SLIC circuit. The method includes periodically switching an applied current from one to the other of the terminals of the two-wire interface and adjusting the gain of at least one of the said signal paths in response to detected common mode signals induced by the applied current. (Gay, col. 2, lines 18-31).

Chen includes of disclosure of a subscriber line interface circuit having circuit components selectively controllable by a microprocessor to provide normal BORSCHT functions or to be selectively tested without the need for an electromechanical relay to isolate the line circuit from the loop conductors. (Chen, col. 2, lines 6-11; Fig. 1)

VII. ISSUES PRESENTED

ISSUE 1: Whether the claims of Group I were properly rejected under 35 U.S.C. § 103

Sub-issue: References alone or combined do not teach or suggest all claim limitations

ISSUE 2: Whether the claims of Group II were properly rejected under 35 U.S.C. § 103

Sub-issue: References alone or combined do not teach or suggest all claim limitations

VIII. GROUPING OF CLAIMS

Claims 1-13, 21-27, and 32-36 stand together (Group I)

Claims 15-20 stand together (Group II)

IX. ARGUMENT

Claim 1-13, 15-17, and 32-36 (Groups I, II) were rejected under 35 U.S.C. § 103 in view of various combinations of Zhou, Warner, Smith, Gay, and Chen. In order to sustain a rejection under 35 U.S.C. § 103, three criteria must be met:

> *First*, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Second*, there must be a reasonable expectation of success. *Finally*, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure

(*In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991)(*emphasis added*)

Appellant respectfully submits that the Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103 and therefore the claims of Groups I and II were improperly rejected under 35 U.S.C. § 103 in view of the cited references.

ISSUE 1: Whether the claims of Group I were improperly rejected under 35 U.S.C. § 103.

Sub-issue: References alone or combined do not teach or suggest all claim limitations

Appellant respectfully submits that *none of the cited references alone or combined teaches or suggests incorporating a codec within the same integrated circuit as a signal processor that provides linefeed driver control signals in response to tip and ring signals sensed by the signal processor.*

With respect to the rejection of claims 1-2, the Examiner has stated:

> Zhou teaches a subscriber loop interface circuit (i.e., line card 308 as shown in figure 3) comprising:
>
> a signal processor (i.e., Digital Signal Processor 304 or DSP 508 shown in figure 5A) having sense inputs for sensed tip signal and a sense ring signal of a subscriber loop (col. 5, lines 27-42 and col. 6, lines 5-29), wherein the signal processor generates a linefeed driver control signal in response to the sensed signals, wherein the signal processor resides on an integrated circuit die (col. 6, lines 34-51).

(12/12/2003 Final Office Action, pp. 2-3)

Appellant respectfully submits that Zhou's tip and ring signals are sensed by circuitry (SLIC 310) other than the digital signal processor 304. (Zhou, col. 6, lines 3-13). Referring to Figures 3, 5A, and 5B, for example, Zhou's tip and ring lines are sensed by the XASLIC (504). The sensed data is then sampled by A/D converters such as converter 506 to produce a digital signal. The digital signal is then provided to the DSP 508 (Zhou, col. 6, lines 5-51; col. 7, lines 11-53; Figs. 3, 5A, 5B). *Thus Zhou's DSP never senses the tip and ring lines.* To the contrary, Zhou's DSP is isolated from the tip and ring lines by the XSLIC and converter circuitry. At best the DSP receives a sampled version of the data sensed by the SLIC.

With respect to Warner the Examiner further states:

> The SLIC further comprises an integrated circuit such as XBRID module 100. The XBRID module 100 includes HVLI 101 and HCOMBO 102 (col. 5, lines 31-53). The HCOMBO further functions as a CODEC for a purposes of performing analog-to-digital and digital-to-analog conversion (col. 8, lines 56-col. 9, lines 7; col. 16, lines 34-64)

(12/12/2003 Final Office Action, p. 3)

Appellant agrees that HCOMBO performs the CODEC functions (see, Warner, col. 8, lines 56-63), however, appellant respectfully submits that XBRID module 100 is not an integrated circuit. HVLI 101 is indicated as being a bipolar *monolithic integrated circuit incorporating the components indicated by broken line 105 illustrated in Figure 3.* (Warner, col. 5, line 63- col. 6, line 8; Fig. 3). HCOMBO 102 is indicated as being a *monolithic integrated circuit incorporating the components illustrated by broken line 105 illustrated in Figure 4.* (Warner, col. 8, line 63-col. 9, line 2; Fig. 4). Clearly, HCOMBO and HVLI are distinct integrated circuits (see, e.g., Warner, col. 6, lines 51-52). If HCOMBO and HVLI are distinct monolithic integrated circuits, then XBRID 100 cannot be an integrated circuit as proposed by the Examiner.

Appellant further notes that HCOMBO does not generate the linefeed control signals, nor does HCOMBO sense the tip and ring lines. To the contrary, the tip and ring lines are sensed by HVLI. HVLI provides the sensed data to line control interface circuits (104) that perform the control and sense logic functions

in conjunction with a peripheral processor 20 that does not even reside on the same line card, much less within a same integrated circuit. (Warner, col. 3, lines 39-56; col. 12, lines 42-53; Figs. 1, 2, see also detail of HVLI in Fig. 3).

With respect to claim 3, the Examiner cited Smith as being combinable with Zhou and Warner to teach that the "signal processor" could be a CMOS signal processor. As previously discussed, appellant respectfully submits, that the integrated circuit of Warner that performs the tip and ring line sensing is in fact a bipolar monolithic integrated circuit presumably due to the high voltage interface functions performed. Given that this reference is only cited with respect to dependent claims, however, this point was only brought forth for clarification.

Gay is cited as teaching that the signal processor calculates common mode and differential mode components of the subscriber loop. Appellant respectfully traverses the Examiner's characterization of Gay. In particular, appellant notes that Gay's microprocessor applies a commutating signal to a common mode simulator to determine a mismatch between two gain elements G1 and G2. The amount of mismatch is proportional to a cumulative voltage resulting from two phases of common mode simulation (Gay, col. 10, lines 2-19). In response to this voltage, the microprocessor sets a programmable attenuator in order to match the effective gains. (Gay, col. 11, lines 14-47; Figs 3, 4). Aside from other distinctions, appellant found no support for the proposition that Gay's microprocessor calculates the common mode or differential mode components of the subscriber line.

With respect to Chen and the rejection of claims 5-8, 11-12, 21, 23, 26, and 32-36, the Examiner has noted that Chen fails to clearly teach the claimed signal processor residing on the same integrated circuit die as a codec, but has relied on Warner for such a limitation. (12/12/2003 Office Action, p. 5) Appellant agrees with the Examiner's observation of Chen's lack of such a teaching and further notes that Warner similarly does not teach such a limitation as already argued above.

Thus none of the cited references, alone or combined, teaches or suggests incorporating a codec within a same integrated circuit as a signal processor that provides linefeed driver control signals in response tip and ring signals sensed by the signal processor.

In contrast, claim 1 includes the language:

> 1. A subscriber loop interface circuit apparatus comprising:
> *a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor generates a linefeed driver control signal in response to the sensed signals, wherein the signal processor resides on a same integrated circuit die as a codec* for bi-directional communication of voiceband data between the analog subscriber loop and a digital interface of the signal processor.

(Claim 1)(*emphasis added*)

> 5. An apparatus comprising:
> *a signal processor generating subscriber loop control signals in response to a sensed tip signal and a sensed ring signal of a subscriber loop*; and
> a linefeed driver portion for driving the subscriber loop in accordance with the subscriber loop control signals, the linefeed driver portion providing the sensed tip and ring signals, wherein each of the linefeed driver portion and the signal processor resides on an integrated circuit die, *wherein the signal processor resides on a same integrated circuit die as a codec* for bi-directional communication of voiceband data between the analog subscriber loop and a digital interface of the signal processor.

(Claim 5)(*emphasis added*)

> 21. A subscriber loop interface circuit apparatus comprising:
> *a signal processor configured to receive a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor generates subscriber loop linefeed driver control signals in response to the sensed tip and ring signals*; and
> *a codec* for converting digital voiceband data to analog voiceband data for the subscriber loop, *the codec and signal processor residing within a same integrated circuit.*

(Claim 21)(*emphasis added*)

Applicant thus respectfully submits claims 1, 5, and 21 are patentable under 35 U.S.C. § 103 in view of the cited references. Given that claim 2-4 depend from claim 1, claims 6-14 depend from claim 5, and claims 22-36 depend from claim 21, appellant respectfully submits claims 2-4, 6-14, and 22-36 are

likewise patentable under 35 U.S.C. § 103 in view of the cited references. Accordingly, appellant respectfully submits all the claims of Group I are patentable under 35 U.S.C. § 103.

ISSUE 2: Whether the claims of Group II were properly rejected under 35 U.S.C. § 103.

Sub-issue: References alone or combined do not teach or suggest all claim limitations

The Examiner has rejected the claims of Group II based on Chen, Warner, and Gay. As noted above, a *prima facie* case of obviousness under 35 U.S.C. § 103 will fail to have been made if the prior art reference (or references when combined) fail to teach or suggest all the claim limitations.

Appellant respectfully submits none of the cited references teaches or suggests *a codec residing within a common integrated circuit with a signal processor that senses the tip and ring lines of a subscriber loop, wherein the signal processor computes common mode and differential mode components of the subscriber loop.*

The Examiner has relied upon Chen for teaching a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop; Gay for teaching a signal processor computing common mode and differential mode components of the subscriber loop; and Warner for teaching the signal processor residing on the same integrated circuit die as the codec. (12/12/2003 Office Action, pp. 9-10).

With respect to Chen, the Examiner has stated that Chen teaches:

> a signal processor (i.e., microprocessor/digital signal processor DSP) having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop (col. 5, lines 65- col. 6, line 24; col. 9, lines 37-67; col. 10, lines 2-7).

(12/12/2003 Office Action, p. 9)

Appellant respectfully traverses the Examiner's characterization of Chen. Referring to Figure 1, and the cited text - the Examiner is referring to outputs of the codec/signal processor - not inputs. The sensing described is being performed by external amplifiers for feedback control. The described sensing is

not performed by the codec/signal processor. The inputs to the DSP include the codec, NADET, and NLC (Chen, col. 5, lines 12-23).

Neither NRDET nor NLC correspond to either a sensed tip or a sensed ring signal. NLC is a logic value (i.e., high/low) that does not correspond to either the sensed tip or the sensed ring line (Chen, col. 5, lines 1-11; col. 9, lines 37-57).

NRDET is similarly a logic value indicating whether the microprocessor should trip ringing based on the off-hook status of the subscriber line. (Chen, col. 5, lines 47-63). NRDET does not correspond to either a sensed tip or a sensed ring signal.

Chen's DSP receives digital values from the codec corresponding to a differential analog signal appearing on the subscriber line. Even if the codec could be said to have tip and ring sense inputs, Chen's DSP signal processor does not. There is no teaching or suggesting that the digital value provided by the codec to the DSP represents any of a sensed ring signal or a sensed tip signal.

As already noted above with respect to the arguments presented in support of Group I: Gay does not teach or suggest a signal processor computing common mode and differential mode components of the subscriber loop. Gay's microprocessor varies the effective gain of at least one of the output stages for the tip and ring lines during a common mode simulation in response to a voltage V_{OAB} that corresponds to a mismatch in the output stage gains. Appellant submits there is no explicit support for the proposition that Gay's microprocessor must calculate differential or common mode components in order to vary the effective gain in response to V_{OAB} nor is such a calculation implicitly required. (Gay, col. 10, lines 2-19; col. 11, lines 14-47).

Although Warner's HVLI senses the tip and ring lines, Warner's HCOMBO does not appear to sense either the ring or tip lines. HCOMBO receives the differential signal VFTX-, VFTX+ from HVLI which does not correspond to either the sensed ring or the sensed tip signal. (see, e.g., Warner, Figs. 3, 4). Thus although XBRID 100 could be said to sense the tip and ring lines,

XBRID 100 is not an integrated circuit. If the integrated circuit HCOMBO residing on XBRID is analogized to appellant's signal processor in an attempt to meet the claimed codec limitation, appellant submits that HCOMBO fails to meet the limitation of sensing the tip and ring lines of the subscriber loop.

Thus none of the cited references teaches or suggests *a codec residing within a common integrated circuit with a signal processor that senses the tip and ring lines of a subscriber loop, wherein the signal processor computes common mode and differential mode components of the subscriber loop.*

In contrast, claim 15 includes the language:

> 15. A subscriber loop interface circuit apparatus comprising:
> *a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor computes common mode and differential mode components of the subscriber loop;* and
> *a codec* for converting digital voiceband data from a digital voiceband interface of the signal processor to analog voiceband data for communicating to the subscriber loop, the codec providing bi-directional voiceband data conversion between the analog subscriber loop and the digital voiceband interface of the signal processor, *the codec and signal processor residing within a common integrated circuit.*

(Claim 15)(*emphasis added*)

Thus appellant respectfully submits claim 15 is patentable under 35 U.S.C. § 103 in view of the cited references. Given that claims 16-20 depend from claim 15, appellant respectfully submits claims 16-20 are likewise patentable under 35 U.S.C. § 103 in view of the cited references. Accordingly, appellant respectfully submits all the claims of Group II are patentable under 35 U.S.C. § 103 and that the rejection of the claims of Group II is improper.

X. CONCLUSION

Appellant respectfully submits that the stated rejections cannot be maintained in view of the arguments set forth above. The Examiner has failed to establish even a *prima facie* case of obviousness under 35 U.S.C. § 103 in view of the cited references for the claims of either Group I or Group II. Thus the claims

of Groups I and II are patentable under 35 U.S.C. § 103 in view of the cited references.

Appellant respectfully requests that the Board of Patent Appeals and Interferences direct allowance of the rejected claims 1-13, 21-27, and 32-36 (Group I), and rejected claims 15-20 (Group II), such that all of pending claims 1-36 are allowed.

If there are any issues that can be resolved by telephone conference, the undersigned representative of the appellant may be contacted at **(512) 306-9470 OR (512) 858-9910.**

Respectfully submitted,

Date: October 14, 2004

William D. Davis
Reg. No. 38,428

APPENDIX I

The claims and their status are presented below.

1. (PREVIOUSLY PRESENTED) A subscriber loop interface circuit apparatus comprising:

a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor generates a linefeed driver control signal in response to the sensed signals, wherein the signal processor resides on a same integrated circuit die as a codec for bi-directional communication of voiceband data between the analog subscriber loop and a digital interface of the signal processor.

2. (ORIGINAL) The apparatus of claim 1 wherein the sensed tip signal includes first and second sensed tip voltages, wherein a difference between the first and second sensed tip voltages is proportional to a tip current, wherein the sensed ring signal includes first and second sensed ring voltages, wherein a difference between the first and second sensed ring voltages is proportional to a ring current.

3. (ORIGINAL) The apparatus of claim 1 wherein the signal processor is a complementary metal oxide semiconductor (CMOS) integrated circuit.

4. (ORIGINAL) The apparatus of claim 1 wherein the signal processor calculates common mode and differential mode components of the subscriber loop.

5. (PREVIOUSLY PRESENTED) An apparatus comprising:

a signal processor generating subscriber loop control signals in response to a sensed tip signal and a sensed ring signal of a subscriber loop; and

a linefeed driver portion for driving the subscriber loop in accordance with the subscriber loop control signals, the linefeed driver portion providing the

sensed tip and ring signals, wherein each of the linefeed driver portion and the signal processor resides on an integrated circuit die, wherein the signal processor resides on a same integrated circuit die as a codec for bi-directional communication of voiceband data between the analog subscriber loop and a digital interface of the signal processor.

6. (ORIGINAL) The apparatus of claim 5 wherein the signal processor and the linefeed driver portion reside on a same integrated circuit die.

7. (ORIGINAL) The apparatus of claim 5 wherein the signal processor and the linefeed driver portion reside on separate integrated circuit die in separate integrated circuit packages.

8. (ORIGINAL) The apparatus of claim 5 wherein the signal processor and the linefeed driver portion reside on separate integrated circuit die within a same integrated circuit package.

9. (ORIGINAL) The apparatus of claim 5 wherein the integrated circuit die is a complementary metal oxide semiconductor (CMOS) integrated circuit.

10. (ORIGINAL) The apparatus of claim 5 wherein the signal processor computes common mode and differential mode components of the subscriber loop.

11. (ORIGINAL) The apparatus of claim 5 wherein the linefeed driver portion comprises:

power circuitry providing battery feed to a ring node and a tip node of the subscriber loop in accordance with the subscriber loop control signals; and

sense circuitry providing the sensed tip and ring signals, wherein the sensed tip and ring signals correspond to a tip current and a ring current of the subscriber loop.

12. (ORIGINAL) The apparatus of claim 11 wherein the sense circuitry comprises:

a tip resistor series-coupled to the tip node and the power circuitry;

a pair of tip sampling resistors one end of each tip sampling resistor connected to opposite ends of the tip resistor, the other end of each tip sampling resistor forming a tip sense node;

a ring resistor series-coupled to the ring node and the power circuitry;

a pair of ring sampling resistors one end of each ring sampling resistor connected to opposite ends of the ring resistor, the other end of each ring sampling resistor forming a ring sense node.

13. (ORIGINAL) The apparatus of claim 11 wherein the sensed tip signal comprises first and second sensed tip voltages, wherein a difference between the first and second sensed tip voltages is proportional to the tip current, wherein the sensed ring signal includes first and second sensed ring voltages, wherein a difference between the first and second sensed ring voltages is proportional to the ring current.

14. (ORIGINAL) The apparatus of claim 11 wherein the power circuitry comprises:

a tip control circuit, wherein the tip control circuit increases a tip node voltage in response to a first tip control signal, wherein the tip control circuit decreases a tip node voltage in response to a second tip control signal; and

a ring control circuit wherein the ring control circuit increases a ring node voltage in response to a first ring control signal, wherein the ring control circuit decreases a ring node voltage in response to a second ring control signal.

15. (PREVIOUSLY PRESENTED) A subscriber loop interface circuit apparatus comprising:

a signal processor having sense inputs for a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor computes common mode and differential mode components of the subscriber loop; and

a codec for converting digital voiceband data from a digital voiceband interface of the signal processor to analog voiceband data for communicating to the subscriber loop, the codec providing bi-directional voiceband data conversion between the analog subscriber loop and the digital voiceband interface of the signal processor, the codec and signal processor residing within a common integrated circuit.

16. (ORIGINAL) The apparatus of claim 15 further comprising:

a linefeed driver portion for driving the subscriber loop in accordance with subscriber loop control signals provided by the signal processor, the linefeed driver portion providing the sensed tip and ring signals.

17. (PREVIOUSLY PRESENTED) The apparatus of claim 16 wherein each of the signal processor and the linefeed driver portion resides on an integrated circuit die.

18. (ORIGINAL) The apparatus of claim 16 wherein the signal processor and the linefeed driver portion reside on separate integrated circuit die within a same integrated circuit package.

19. (ORIGINAL) The apparatus of claim 16 wherein the signal processor and the linefeed driver portion reside on a same integrated circuit die.

20. (ORIGINAL) The apparatus of claim 16 wherein each of the signal processor and the linefeed driver portion resides on separate integrated circuit die in separate integrated circuit packages.

21. (PREVIOUSLY PRESENTED) A subscriber loop interface circuit apparatus comprising:

a signal processor configured to receive a sensed tip signal and a sensed ring signal of a subscriber loop, wherein the signal processor generates subscriber loop linefeed driver control signals in response to the sensed tip and ring signals; and

a codec for converting digital voiceband data to analog voiceband data for the subscriber loop, the codec and signal processor residing within a same integrated circuit.

22. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor computes common mode and differential mode current and voltage components of the subscriber loop.

23. (PREVIOUSLY PRESENTED) The apparatus of claim 21 further comprising:

a linefeed driver for controlling the subscriber loop in response to the linefeed driver control signals, wherein the linefeed driver does not reside within a same integrated circuit as the signal processor.

24. (PREVIOUSLY PRESENTED) The apparatus of claim 23 wherein the linefeed driver does not compute any common mode subscriber loop voltages or currents, wherein the linefeed driver does not compute any differential mode voltages or currents of the subscriber loop.

25. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor is a complementary metal oxide semiconductor (CMOS) integrated circuit.

26. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor operates in a positive voltage range with respect to ground to generate the linefeed driver control signals for controlling a linefeed driver operating at a negative d.c. voltage offset relative to the signal processor, wherein the offset is at least approximately 40 VDC.

27. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the sensed tip signal includes first and second sampled tip voltages, wherein a difference between the first and second sampled tip voltages is proportional to a subscriber loop tip current, wherein the sensed ring signal includes first and second sampled ring voltages, wherein a difference between the first and second sampled ring voltages is proportional to a subscriber loop ring current.

28. (PREVIOUSLY PRESENTED) The apparatus of claim 23 wherein the linefeed driver further comprises:

a tip control circuit; and

a ring control circuit, wherein the tip and ring control circuits vary tip and ring node voltages of the subscriber loop in response to the linefeed driver control signals.

29. (PREVIOUSLY PRESENTED) The apparatus of claim 28 wherein the tip and ring control circuits provide d.c. isolation between the signal processor and the subscriber loop.

30. (PREVIOUSLY PRESENTED) The apparatus of claim 28 wherein the tip control circuit further comprises:

a first transistor of a first type having an emitter coupled to receive a first tip control signal of the linefeed driver control signals;

a second transistor of a first type having an emitter coupled to receive a second tip control signal of the linefeed control signals, wherein a base of the first and second transistors is coupled to a common signal ground node;

a third transistor of a second type having a collector coupled to a collector of the first transistor and a tip line of the subscriber loop;

a resistor having a first end coupled to the emitter of the third transistor to form a battery feed node, wherein a second end of the resistor coupled to a base of the third transistor and a collector of the second transistor.

31. (PREVIOUSLY PRESENTED) The apparatus of claim 30 wherein the first type is a PNP bipolar junction transistor, wherein the second type is an NPN bipolar junction transistor.

32. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor performs at least one of the subscriber loop supervisory functions of ring trip, ground key, and off-hook detection.

33. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor performs subscriber loop ring control, supervision, codec, and hybrid functions.

34. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor further comprises a programming interface to enable programmatic control of at least one of the following parameters: battery control, battery feed state control, voiceband data amplification, voiceband data level shifting, longitudinal balance, ringing current, ring trip detection threshold, off-hook

detection threshold, and audio output signal termination impedance for voiceband communication signals superimposed on the linefeed driver control signals.

35. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the signal processor superimposes outgoing analog voiceband communications on the linefeed driver control signals.

36. (PREVIOUSLY PRESENTED) The apparatus of claim 21 wherein the linefeed driver control signals include separate tip control signals and ring control signals.